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H3A

Selected US specifications from IPC sub-classes H03B H03L H03K

(54) Phase-locked loop delay line

(57) A circuit for providing precise delays includes a phase-locked loop driven by a reference frequency source such as a crystal oscillator 10 and including a variable delay circuit 12. The output of the oscillator 10 is applied to the delay circuit 12 and the non-delayed and delayed signals are compared in a phase comparator 16. An error signal representative of phase error is developed and applied to vary the amount of delay until the phase error is eliminated. A precise delay referenced to the oscillator frequency is therefore achieved. The delay line 12 is formed of series-connected CMOS inverter pairs.

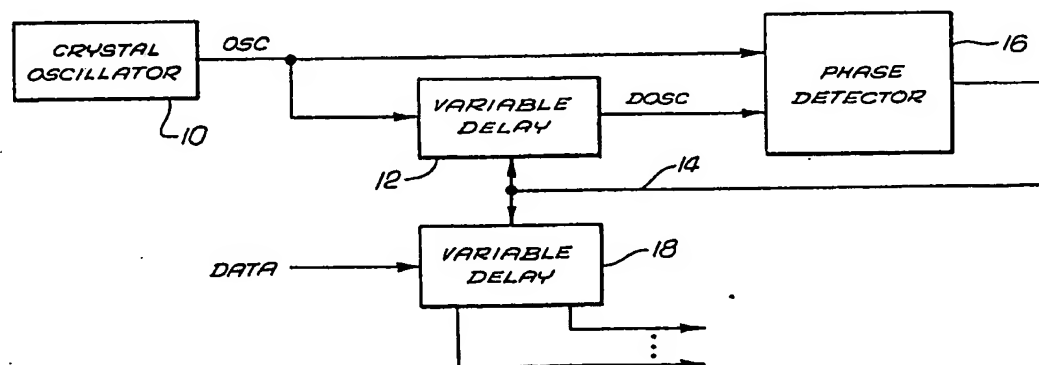


FIG. 1

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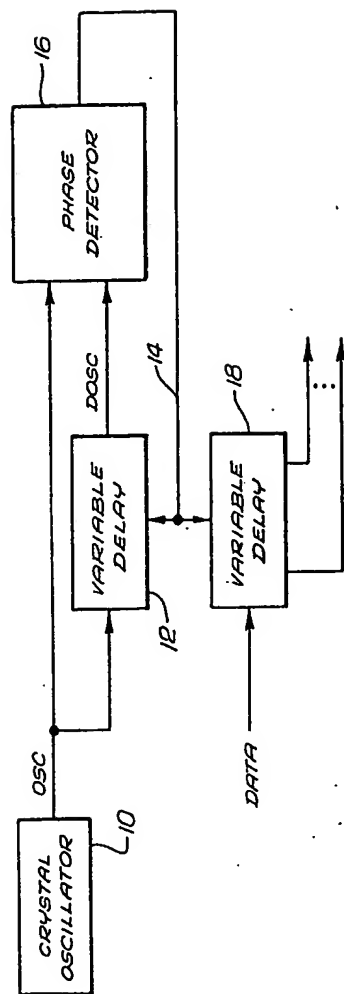


FIG. 1

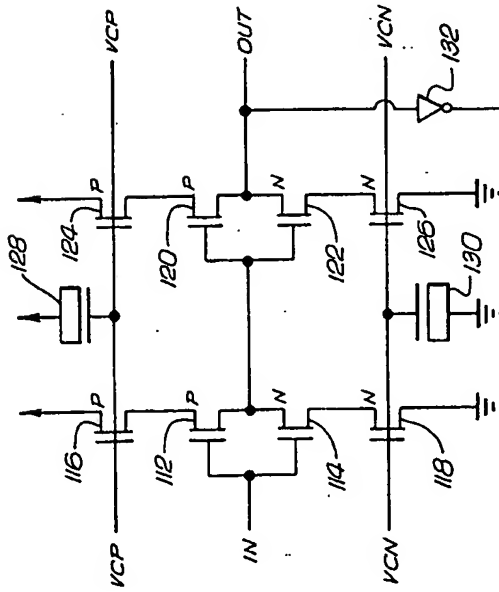


FIG. 3

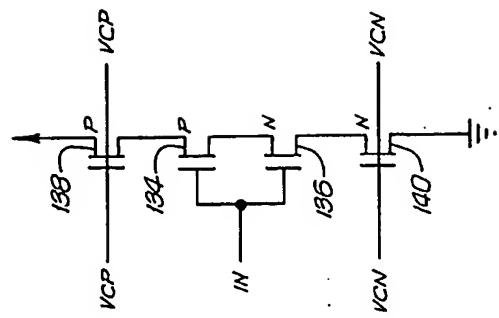
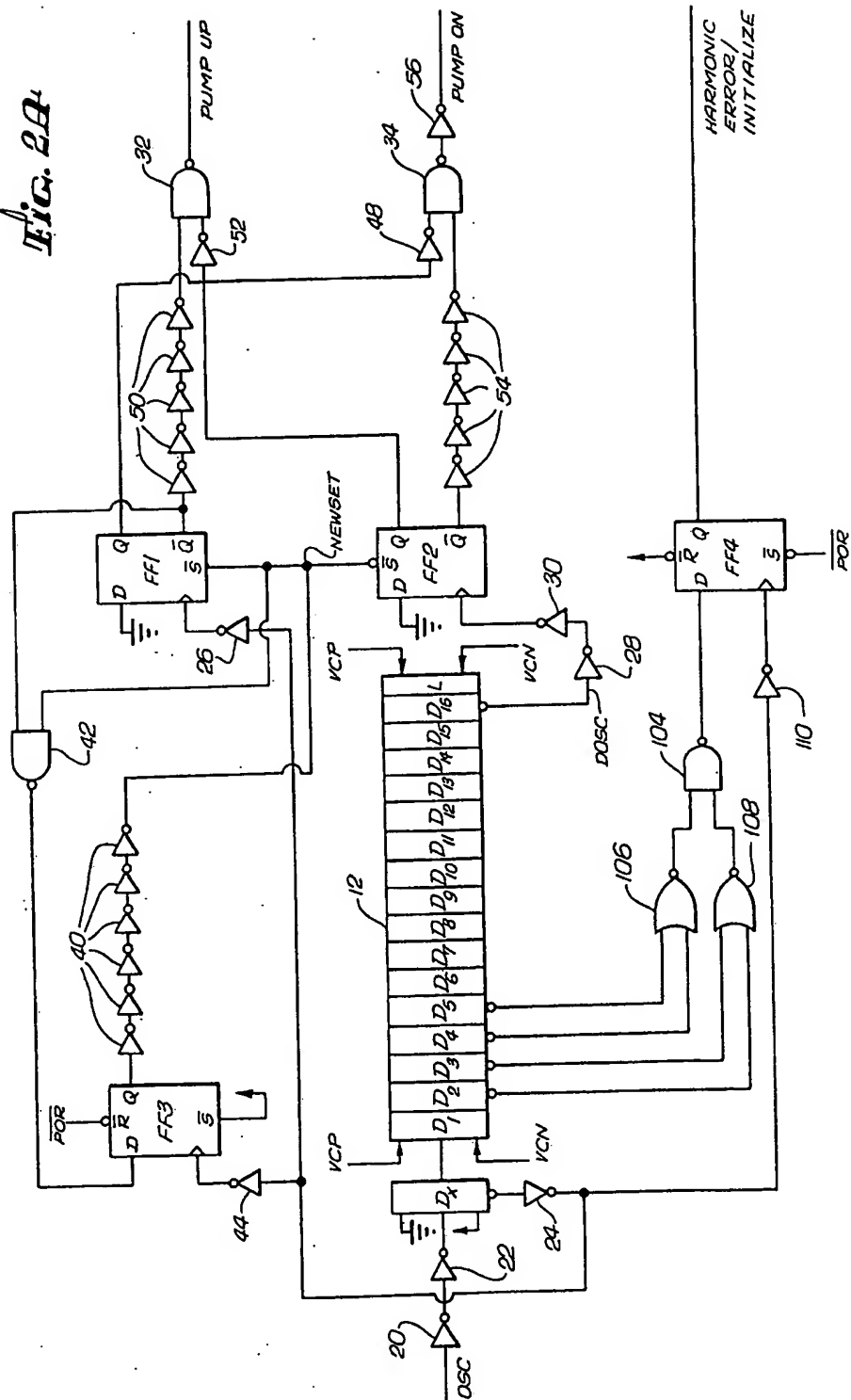
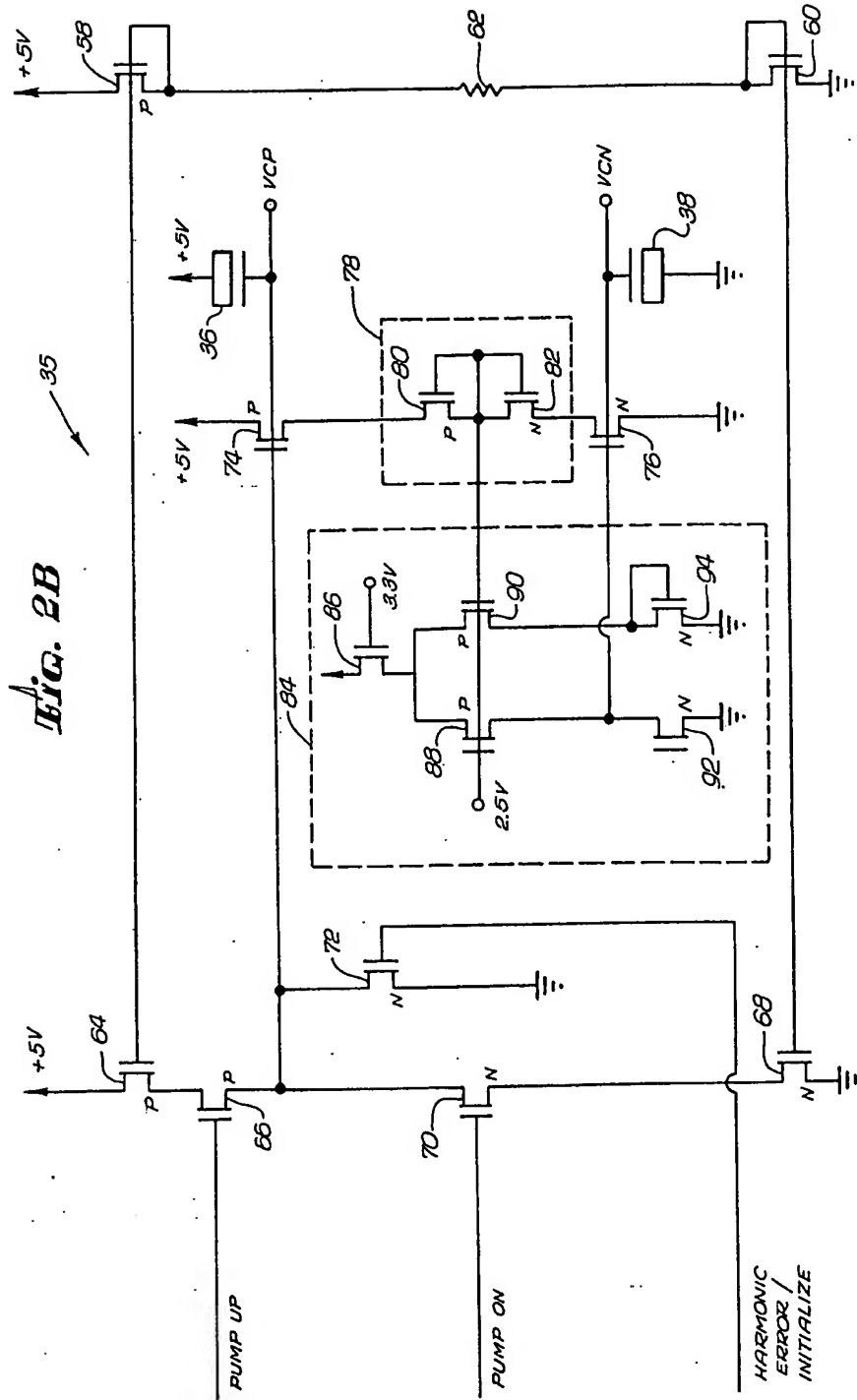


FIG. 4

Fig. 2A





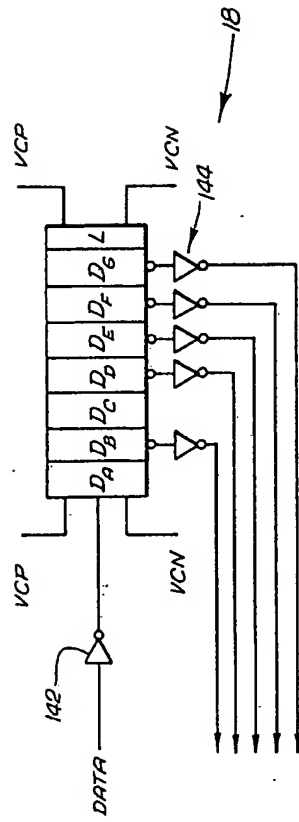


Fig. 5

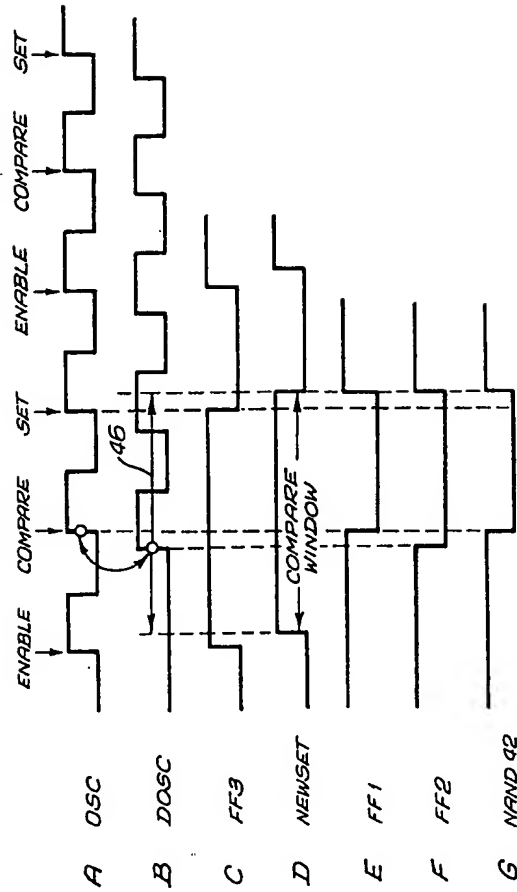


Fig. 6

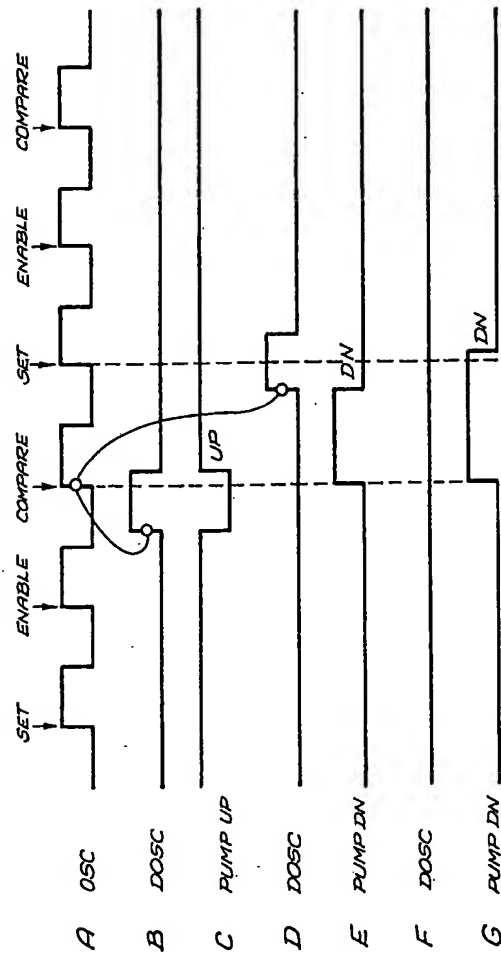


FIG. 7

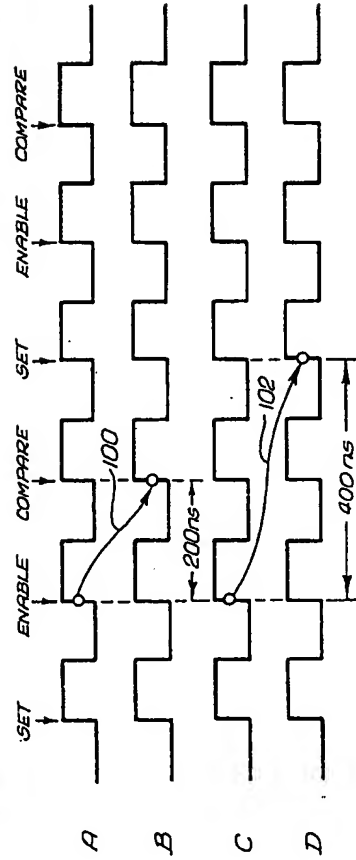


FIG. 8

SPECIFICATION

Phase-locked loop delay line

5 BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a delay circuit for providing an output signal which is delayed by a precise amount with respect to an input signal. Such circuits are typically referred to as "delay lines" and have many applications. For example, delay lines are commonly used in data separator phase-locked loops used in disc drive systems. Delay lines are also used to provide optimum timing for control of high speed dynamic RAM devices, which comprise the main memory of virtually all personal computers.

2. Description of the Prior Art

One type of prior art delay line is formed of a plurality of series-connected circuits such as inverters. Each inverter provides a known amount of delay, and outputs of various delays with respect to each other are derived by tapping the outputs of different inverters along the line. Other types of delay lines include LC circuits and RC circuits. In order to achieve precise delays, parameters which affect the delay, e.g., process, temperature and voltage, must be very tightly controlled. Obtaining accurate delays in integrated circuit delay lines has proven to be extremely difficult. The number of parameters involved, as well as the fact that the parameters change over time, renders it difficult to obtain and maintain a desired delay. Not only is it difficult to obtain precise delays, efforts to do so through tight control of various parameters results in increased fabrication costs for the integrated circuit.

SUMMARY OF THE INVENTION

The present invention is directed to a delay line which incorporates a phase-locked loop in order to obtain and maintain precise delays. The invention takes advantage of the fact that although integrated circuit delays in and of themselves are not very accurate, the delay through identical structures (such as inverter pairs) is extremely well matched. The delay line of the present invention incorporates a plurality of matched variable delay circuits which function analogous to a voltage controlled oscillator in a phase-locked loop circuit. The output of a reference frequency source (typically a crystal oscillator of fixed frequency but possibly a variable source such as a voltage controlled oscillator) is applied to the input of the delay line. A phase detector is provided to compare the phase of the output of the delay line with the phase of the input of the delay line. An error signal is generated representative of the phase error and is applied to a control input of the delay line to vary the amount of delay and eliminate the

phase error. When there is no phase error, the delay line is providing a delay equal to an integral number of periods of the reference frequency. Circuitry may be included for ensuring that the delay is equal to a single period of the reference frequency. If the reference frequency is extremely accurate (as will be the case when a crystal oscillator is used), the resulting delay provided by the delay line will also be accurate. Varying parameters such as voltage and temperature changes which may affect the delay line will thus be compensated for, since the phase-locked loop circuit will always cause the control signal to the delay line to be modified to provide the desired delay.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be discussed with reference to the accompanying drawings, wherein: Figure 1 is a block diagram of the present invention;

Figures 2A and 2B are schematic diagrams of portions of the circuit of the present invention;

Figure 3 is a schematic diagram of a single delay block of the delay line;

Figure 4 is a schematic diagram of a final element of the delay line;

Figure 5 is a schematic diagram of the delay line to which a data signal is applied; and

Figures 6-8 are timing diagrams associated with the operation of the delay line of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Fig. 1, the present invention employs a highly accurate periodic signal from a crystal oscillator 10 to provide a delay line with precise desired delays. A variable frequency source such as a voltage controlled oscillator may be employed for certain applications. The output of the oscillator 10 is designated OSC. The output of the oscillator is applied to a variable delay line 12, which provides a delayed output signal DOSC in response to the signal OSC. The amount of delay provided by the circuit 12 is controlled by a control signal received on line 14.

The signals OSC and DOSC are both applied to a phase detector 16 which provides an error signal on the line 14 in response to the detection of a phase difference between the two signals. Thus, unless the DOSC signal is delayed with respect to the OSC signal by precisely one or more periods of the OSC signal, a phase error will exist and an error signal will be generated on the line 14. The amount of delay will be varied in response to the error signal. The phase detector 16 may also include harmonic error detection circuitry to ensure that the delay is equal to a single period of the signal OSC rather than multiple periods.

Thus, the oscillator 10, variable delay line

12 and phase detector 16 form a phase-locked loop circuit which functions to cause the delay line 12 to provide a delay which is precisely equal to one clock period of the output of the oscillator. The control signal on line 14 which is used to control the amount of delay may then be provided to a second delay line 18 which has the same circuitry as the delay line 12 and will therefore provide identical delays. The delay line 18 provides multiple delay output taps, each having a different delay, which can be used to provide desired delays of a data signal labeled DATA. For example, when used in a data separator, the delay line 18 can be used to provide write precompensation and to generate the window signals used for data separation. For certain applications, the delay line 12 can be employed to provide plural control signals of a predetermined relationship. In such applications, the delay line 18 would not be employed.

The operation of a specific embodiment of the present invention will be described with reference to Figs. 2A and 2B. The delay line 12 is formed of a plurality of series-connected blocks D1-D16 and an end block L. Each delay block D is formed of a CMOS inverter pair having modulated current sources to vary its switching speed. Control signals VCP and VCN are applied to each of the blocks to modulate the application of current to the CMOS inverters and vary the switching speed, thus varying the delay provided by the overall delay line.

The OSC signal from the oscillator is applied to the delay line via buffer inverters 20 and 22 and an initial delay block Dx which is provided for waveform shaping to ensure that each block of the delay line will be operating on an identically shaped signal so that the delay through each block will be identical.

The basic phase detection operation to detect a phase error between the oscillator and the output of the delay line 12 is accomplished by means of D-type flip-flops FF1 and FF2. The flip-flop FF1 is clocked by the OSC signal (applied through the inverters 20 and 22, the block Dx, an inverter 24 and an inverter 26, the delays of which are ignored in the discussion of the circuit operation). The DOSC signal clocks the flip-flop FF2 through inverters 28 and 30 (matching the delays through inverters 24 and 26). The inverters 24, 26, 28 and 30 serve as buffers to the inputs of the flip-flops.

The outputs of the flip-flops FF1 and FF2 drive two NAND gates 32 and 34, the outputs of which are applied to a charge pump 35 illustrated in Fig. 2B. The charge pump generates the control signals VCP and VCN. Depending on the outputs of the NAND gates 32 and 34, MOS capacitors 36 and 38 in the charge pump will be charged or discharged to vary the values of control voltages VCP and

VCN. These control voltages are applied to the delay circuit 12 to vary the amount of delay which is provided by each block. The shortest delay is provided when VCP is zero volts.

The present invention employs an additional D-type flip-flop FF3 and associated control circuitry to provide a three cycle phase comparison sequence which ensures that a correct determination will be made as to whether the delayed signal DOSC is leading or lagging the phase of the oscillator signal OSC (methods other than a three cycle sequence may also be employed). Corrections in the control signals VCP and VCN will therefore always be in the proper direction, i.e., to increase the delay when the delayed signal leads the phase of the oscillator signal and decrease the delay when the phase of the delay signal lags the phase of the oscillator signal.

Fig. 6 is a timing diagram illustrating the three cycle phase comparison operation of the circuit of Fig. 2. The circuit is configured so that upon initial application of power, the shortest delay possible will be provided to ensure that the delayed signal will be delayed by less than one period of the OSC signal. The phase locking operation will then cause the delay to be increased until locking occurs with a delay of one period of the OSC signal. Undesirable locking on harmonics (two or more OSC periods) is thus eliminated. The provision of minimum delay upon start-up is accomplished by means of a D-type flip-flop FF4. When power is applied to the circuit a power-on reset pulse \overline{POR} is applied to the set input of the flip-flop FF4, causing its Q output to go high. This signal turns on a transistor 72 (Fig. 2B), causing the capacitor 36 to discharge so that VCP is equal to zero.

The flip-flop FF3 has the power-on reset signal \overline{POR} applied to its reset input. This causes its Q output to go low upon the application of power to the circuit. Six inverters 40 are connected to this output, and the output of the final inverter, labeled NEWSET, is also zero. This signal is applied to the set inputs of flip-flops FF1 and FF2 and to one input of a NAND gate 42. The \overline{Q} output of the flip-flop FF1 is applied to the other input of the NAND gate 42.

The NEWSET signal functions to control the enablement of the flip-flops FF1 and FF2. Initially, NEWSET is low, causing the Q outputs of the flip-flops FF1 and FF2 to be held high. The output of the NAND gate 42 will therefore also be high. When the first rising edge of the OSC signal arrives (labeled "enable" in Fig. 6), it will clock the flip-flop FF3 (via the inverters 20 and 22, delay block Dx, inverter 24 and an inverter 44), passing the high signal at the data input to the Q output. The flip-flop FF1 will not be clocked by the first rising edge of the OSC signal, since it is not enabled due to the NEWSET signal being low.

After a slight delay caused by the inverters 40, the NEWSET signal will go high, thereby enabling both of the flip-flops FF1 and FF2. The flip-flops are thus free to be clocked by the next rising edge of the signals applied to their respective clock inputs. The flip-flop FF1 will be clocked by the OSC signal and the flip-flop FF2 will be clocked by the DOSC signal. Thus, the first OSC signal will enable the flip-flops FF1 and FF2 by means of the action of the flip-flop FF3, thereby allowing the second OSC signal (labeled "compare" in Fig. 6) to clock the flip-flop FF1 and the DOSC signal to clock the flip-flop FF2. The D inputs of both flip-flops are grounded, and the clocking will therefore cause their Q outputs to go low. In Fig. 6 the DOSC signal is illustrated as arriving before the second OSC signal, and the flip-flop FF2 will therefore be clocked first. When the flip-flop FF1 is clocked, its \bar{Q} output will go high and the NAND gate 42 will go low. The next OSC signal (labeled "set" in Fig. 6) will thus cause the Q output of the flip-flop FF3 to go low which, after a short delay through the inverters 40, causes the signal NEWSET to go low. This causes the Q outputs of the flip-flops FF1 and FF2 to go high. The flip-flops will again be enabled by the next OSC pulse (also labeled "enable" in Fig. 6).

Thus, the NEWSET signal provides a window, shown in Fig. 6 as a "compare window", in which the phase comparison between the signals OSC and DOSC is enabled. The window is begun shortly after the occurrence of a first rising edge of the OSC signal to enable the next rising edge of the OSC signal to be phase compared with the delayed signal DOSC. The window is terminated in response to the third rising edge of the OSC signal and the cycle is then repeated. The window generation ensures that the delayed signal DOSC will be compared to the next rising edge of the OSC signal rather than the rising edge corresponding to the delayed signal (e.g., in Fig. 6 the first DOSC edge is compared to the "compare" edge of the OSC signal rather than the "enable" edge which precedes it). In this manner, a correct determination of the direction of any phase error will be made.

The inverters 40 are included to provide a delay in the generation of the NEWSET signal (which is less than the minimum delay through delay element 12) in order to accommodate small amounts of jitter in the DOSC signal. The inclusion of this slight delay further minimizes the chances of incorrectly determining the direction of any phase error.

The actual phase comparison operation performed by the circuit of Fig. 2 for different signals will be described with reference to Fig. 7. The OSC signal is shown in Fig. 7A with the three cycles of "set", "enable" and "compare" labeled. The Q output of the flip-

flop FF1 is applied to the NAND gate 34 via an inverter 48, whereas the \bar{Q} output of the flip-flop FF1 is applied to an input of NAND gate 32 via five inverters 50. Similarly, the Q output of the flip-flop FF2 is applied to an input of the NAND gate 32 via five inverters 52 whereas the \bar{Q} output of the flip-flop FF2 is applied to an input of the NAND gate 34 via five inverters 54. The inverters 50 and 54 serve to provide a slight delay to prevent a dead zone in the operation of the charge pump.

The situation in which the delayed signal DOSC leads the phase of the oscillator signal OSC is illustrated in Fig. 7B. In this situation, the rising edge of the DOSC signal will clock the flip-flop FF2, causing the output of the NAND gate 32 to go low. This output is labeled PUMP UP in Fig. 2 and is shown in Fig. 7C. The low output of the NAND gate 32 causes the charge pump to operate to charge the capacitor 36 and increase the voltage VCP, thereby increasing the amount of delay. Concurrently, the control voltage VCN on the capacitor 38 will be reduced. The specific functioning of the charge pump will be discussed subsequently. When the "compare" OSC signal arrives, the \bar{Q} output of the flip-flop FF1 will go high which, after the delay through the inverters 50, will cause the PUMP UP signal to return to a high level as illustrated in Fig. 7C.

Fig. 7D illustrates the situation in which the delayed signal lags in phase with respect to the OSC signal. In this case the charge pump is discharged to lower the VCP voltage on the capacitor 36. This results in an increase in the voltage on the capacitor 38 and thus the voltage VCN. The "compare" OSC signal will clock the flip-flop FF1, causing its Q output to go low, thus causing the output of the NAND gate 34 to go low. The output of an inverter 56, labeled PUMP DN in Fig. 2 and shown in Fig. 7E, thus goes high and is applied to the charge pump. This signal causes the capacitor 36 to discharge, thus lowering VCP and raising VCN. The lowering of VCP decreases the delay of the DOSC signal, thus causing its phase to catch up with that of the OSC signal.

If for some reason the delayed signal does not occur, as illustrated in Fig. 7F, the circuit will operate to cause the PUMP DN signal to go high to lower the voltage VCP and therefore decrease the delay of the delayed signal. As illustrated in Fig. 7G, the PUMP DN signal will go high at the "compare" edge of the OSC signal and will be reset to a low level at the "set" edge (after the slight delay due to the inverters 54). A new comparison cycle will therefore begin with the shortest delay.

The present invention is designed to track changes in the delay of the delay circuit which are relatively long term and caused by factors such as temperature and supply voltage changes. The three cycle phase comparison

operation which is employed to ensure that the direction of phase errors will be properly determined is sufficiently fast to correct for such long term phase errors occurring in the system.

In a conventional phase-locked loop circuit, frequency differences between the signals whose phases are compared (a reference frequency and a voltage controlled oscillator output) enable phase and frequency locking to eventually be achieved even if initial phase corrections are made in the wrong direction. In the delay circuit of the present invention, the frequencies of the signals being compared are exactly the same, since they originate from the same source. If phase corrections are made in the wrong direction, phase-locking cannot be achieved to result in the proper amount of delay. It is for this reason that a multiple cycle phase comparison sequence is employed to ensure that all phase corrections are in the proper direction.

The operation of the charge pump will be described with reference to Fig. 2B, in which the conductivity of the various MOSFET transistors is indicated by a "P" or "N". The charge pump operates to charge the capacitor 36 in response to the PUMP UP signal being low and discharge the capacitor 36 in response to the PUMP DN signal being high. If neither of these signals is present the voltage on the capacitor 36 (and thus the amount of delay) will remain essentially constant.

The charge pump includes a precision current source formed by two diode connected transistors 58 and 60 and a resistor 62. This provides a reference current for determining the charging and discharging rate of the capacitor 36. The capacitor 36 is charged by means of a transistor 64 coupled to the positive power supply. The transistor 64 is selectively coupled to the capacitor 36 by means of a transistor switch 66 which is rendered conductive when the PUMP UP signal goes low. The transistor 64 is connected to the transistor 58 in a current mirror configuration and the current through the two transistors will therefore be equal. A controlled reference current will therefore be applied to the capacitor 36 in response to the PUMP UP signal going low.

The discharging of the capacitor 36 is controlled in a similar fashion. The discharging is accomplished through a transistor 68 connected in a current mirror configuration to the transistor 60, which is coupled to the capacitor 36 by means of a transistor 70 rendered conductive when the PUMP DN signal is high. Discharging may also occur through the transistor 72 in a manner to be described subsequently.

The charging and the discharging of the capacitor 36 as described above operates to vary the control voltage VCP applied to the variable delay line so as to alter the delay

provided by the circuit. In some applications, the single control voltage may be sufficient to control the delay. However, in the present embodiment of the invention, the second control voltage VCN is also generated and applied to the delay line. As will be discussed in more detail subsequently, the delay line is formed of modulated inverters in which positive and negative supply transistors are modulated to alter the switching time. The voltage VCP is applied to modulate a positive supply transistor and the voltage VCN is applied to modulate a negative supply transistor.

In order to develop VCN from VCP, the circuit of Fig. 2B operates to balance the current through transistors 74 and 76 at a point corresponding to the switching threshold of the inverters of the delay line. This is accomplished by providing an inverter 78, which is modeled after the delay inverters, formed of transistors 80 and 82 and connecting it between the transistors 74 and 76. The input of the inverter is tied to its output and compared to the switching threshold by means of a comparator 84. The switching threshold is set at 2.5 volts, i.e., one-half of the positive power supply voltage of 5 volts. The comparator is formed of transistors 86-94 and will operate to drive the base of the transistor 76 until the input to the base of the transistor 90 is equal to that to the base of the transistor 88, i.e., 2.5 volts. In this manner, the currents through the transistor 74 and 76 are set to be equal at the switching threshold of the inverter 78 (and thus the inverters of the delay line). The voltage applied to the transistor 76 is also applied to charge the capacitor 38 and thus develop the control voltage VCN.

The circuit of Fig. 2 is designed to provide a delay of precisely one period of the OSC signal. In the most common application of the specific embodiment presently used, this period is 200 nanoseconds. Since the phase comparator compares rising edges of the OSC signal and the delayed DOSC signal, however, it is possible that phase-locking could occur on multiples of a single period of the signal OSC. This situation is illustrated in Fig. 8. It is desired that the delay line 12 provide a delay of one clock period as shown in Figs. 8A and 8B. That is, it is desirable that the circuit lock on to the rising edges of the OSC and DOSC signals such that for any two signals being compared the DOSC rising edge was generated by the OSC edge one period previous to the OSC edge being compared. This is illustrated by an arrow 100. However, it is possible that the circuit will actually lock onto a rising edge of the DOSC signal which trails the OSC signal by two or more clock periods, as indicated by an arrow 102 in Figs. 8C and 8D. In such a case, the control voltage VCP and VCN would be improperly controlled such that the modulated inverters of the delay circuit provide a delay of two or more clock

periods of the OSC signal rather than one. It should be noted that even when a circuit provides improper delay, the frequency of the DOSC signal will remain equal to that of the OSC signal since the circuit operates to vary the delay of the OSC signal passing through it but not its frequency.

The present invention includes circuitry to detect improper delays of more than one clock period ("harmonic" errors) and reset the circuit so that it may again provide phase-locking with a delay of a single clock period of the OSC signal. This is accomplished by means of the flip-flop FF4 and logic circuitry including NAND gate 104 and NOR gates 106 and 108 shown in Fig. 2A. Essentially, this circuitry operates to monitor the waveform of the signal passing through the delay line 12 at a particular point in time to ensure that it corresponds to the waveform which would be achieved if the proper delay of a single period of the signal OSC is being provided. If not, the flip-flop FF4 will provide an error signal which will render the transistor 72 shown in Fig. 2B conductive and discharge the capacitor 36. This causes the control voltage VCP to go to zero, thus resetting the circuit to its shortest delay. Any subsequent phase corrections can only increase the amount of delay and the initial phase locking will therefore achieve a single cycle delay. It should be noted that the flip-flop FF4 also renders the transistor 72 conductive when power is first applied to the circuit to start with the shortest delay as previously described. The output of the flip-flop FF4 is thus labeled HARMONIC ERROR/INITIALIZE.

The operation of the delay line 12 is such that a signal will propagate through it with a delay being added at each stage. The overall delay at the final output is equal to the sum of the delays of the various stages. At any point in time, the output of each stage will be at either a high or low level. For example, at the beginning of the OSC pulse, if the proper one cycle delay is being provided, the delay blocks D1-D8 will be at a high level and the blocks D9-D16 at a low level. In contrast, if the overall delay line is providing a two cycle delay, the blocks D1-D4 and D9-D12 will be high and the blocks D5-D8 and D13-D16 will be low. By monitoring the state of different blocks of the delay line at a particular point in time, a determination may be made as to whether the proper delay is being provided. The logic circuitry shown in Fig. 2A provides this function. The flip-flop FF4 is clocked through buffer inverters 24 and 110 by the rising edge of the OSC signal. At this point, the outputs of the delay line blocks D2-D5 should be high and their inverted outputs supplied to the gates 106 and 108 will therefore be low. The output of the NAND gate 104 will therefore also be low and the Q output of the flip-flop FF4 will be low. However, if there

is a harmonic error, the block D5 will be low and its inverted output which is applied to the gate 106 will be high. This will cause the output of the NAND gate 104 to be high, thus causing the Q output of FF4 to go high. This will switch the transistor 72 in Fig. 2B and discharge the capacitor 36. The circuit will then reset to the shortest delay. The phase comparison operation will thus cause the delay to be increased until phase-locking occurs, with the delay at this point being a single cycle of the OSC signal.

Fig. 3 illustrates an individual block D of the delay line 12. Each block is comprised of a pair of CMOS inverters coupled to supply transistors which are modulated by the control signals VCP and VCN. A first inverter includes transistors 112 and 114, with the transistor 112 being coupled to a transistor 116 which is in turn coupled to the positive supply. Similarly, the transistor 114 is coupled to a transistor 118 which is connected to ground. A second inverter includes transistors 120 and 122 coupled to the positive supply and ground by transistors 124 and 126, respectively. MOS capacitors 128 and 130 are provided for local voltage stabilization. By modulating the voltages VCP and VCN, the amount of current supplied to the inverters will be varied, thus varying the switching speed of the inverters. The output of the second inverter is applied to the input of the subsequent delay block and in addition may be provided as a delay line output through a buffer inverter 132. This inverted output is the output applied to the logic circuitry for harmonic detection for the blocks D2-D5 and is the overall delayed output signal DOSC from the block D16.

As shown in Fig. 4, a final block L of the delay line is formed of a single modulated inverter including transistors 134 and 136 and modulated supply transistors 138 and 140. The purpose of this final block is to ensure that the output waveform DOSC is not affected by being the last block in the delay line.

The circuitry of Fig. 2 is provided to develop the control voltages VCP and VCN which will cause the desired delay to be achieved. However, since the OSC signal must be applied to the delay line 12 to enable development of the control voltages, the second delay line 18 is provided to achieve actual delay of a data input signal. This delay line is illustrated in Fig. 5 as including seven delay blocks D_A-D_G which are identical to the blocks in the delay line 12. The control voltages VCP and VCN will therefore provide the blocks D_A-D_G with the same delay as the blocks D1-D16. This amount of delay is, of course, locked on to a desired value by the operation of the phase-locked loop circuit. In the situation where a 200 nanosecond delay is provided by the delay line 12, each block of the

delay lines 12 and 18 will provide a delay of 12.5 nanoseconds. A data signal is applied to the delay line 18 via a buffer inverter 142, and the outputs of various blocks of the line 18 may be employed to provide signals of different desired delays. For example, in order to generate a window signal for data separation, the output of the blocks D_8 and D_6 may be used to provide two signals having a precise delay with respect to each other. In this instance, since the two blocks are five blocks apart, the overall delay would be 60 nanoseconds. Similarly, other outputs may be employed to provide different amounts of delay for write precompensation purposes. Inverters 144 are provided to obtain signals having proper polarity for application to subsequent logic circuitry. It should be noted that the data signal which is applied as the input to the delay line 18 is not used as the non-delayed signal for application to further circuitry. Rather, two of the delayed signals are employed because of the precise known delay between blocks.

In summary, the present invention provides a phase-locked loop delay circuit which achieves precise delays despite changes in operating parameters such as temperature and power supply, and wide variations in processing during circuit manufacture. The system incorporates a variable delay line in a phase-locked loop circuit, with the phase-locking operation being used to generate a control voltage to control the amount of delay provided by the delay line. A separate delay line incorporating identical delay blocks is controlled by the same control voltage and is used to delay a data signal. The invention is especially useful in systems in which a crystal oscillator or other reference timing signal source is already provided in the circuit.

CLAIMS

1. A circuit for providing a signal having a precise delay with respect to a digital input signal, comprising:
 - a reference frequency source for generating a periodic input signal;
 - a variable delay circuit for receiving the input signal and generating an output signal which is delayed with respect to the input signal; and
 - control means for comparing the phase between the input signal and the output signal and varying the amount of delay provided by the delay circuit to achieve a desired phase relationship.
2. A circuit as in claim 1 wherein:
 - the delay circuit includes a control input for receiving a control voltage to control the amount of delay; and
 - the control means includes means for generating the control voltage as a function of the phase difference between the input signal and output signal.
3. A circuit as in claim 2 wherein the control means includes means for determining

whether the phase of the input signal leads or lags the phase of the output signal and varying the control voltage in a first or second direction in response to the determination.

4. A circuit as in claim 3 wherein the means for generating the control voltage includes a charge pump having a capacitor which is charged or discharged, wherein the voltage across the capacitor is the control voltage, wherein the means for determining generates a first signal causing the charge pump to charge the capacitor in a first direction when the phase of the input signal leads the phase of the output signal and generates a second signal causing the charge pump to charge the capacitor in the opposite direction when the phase of the input signal lags the phase of the output signal.

5. A circuit as in claim 4 wherein the means for determining includes a phase detector which receives the input signal and output signal and generates the first signal during a time period between a rising edge of the input signal and the next rising edge of the output signal and generates the second signal during a time period between a rising edge of the output signal and the next rising edge of the input signal.

6. A circuit as in claim 5 wherein the phase detector includes a first D-type flip-flop which is set by a rising edge of the input signal and a second D-type flip-flop which is set by a rising edge of the output signal, a first logic gate operatively coupled to receive an output from each flip-flop and provide said first signal and a second logic gate operatively coupled to receive an output from each flip-flop and provide said second signal.

7. A circuit as in any of claims 1 to 6 including harmonic control means for causing the output signal to be delayed with respect to the input signal by a predetermined number of periods of the input signal.

8. A circuit as in claim 7 wherein the predetermined number of periods is one and wherein the harmonic control means includes means for monitoring the output signal to determine whether it has a desired timing relationship to the input signal and means for correcting the operation of the circuit to achieve a delay of one period if an improper waveform is detected.

9. A circuit as in claim 8 wherein the means for correcting includes means for resetting the delay circuit to provide an output signal having a minimum delay, whereby the circuit will thereafter operate to increase the delay of the output signal to achieve a delay of one period of the input signal.

10. A circuit as in claim 2 or any of claims 3 to 9 when appendant to Claim 2 wherein the delay circuit includes a plurality of series connected inverters and means for modulating the switching speed of the inverters.

11. A circuit as in claim 10 wherein each

inverter is comprised of a CMOS transistor pair and wherein the means for modulating comprises additional transistors coupled between the inverters and power supply connections, wherein the control voltage is applied to the additional transistors to modulate the current supplied to the inverters and thereby modulate their switching speed.

12. A phase-locked circuit for providing an output signal having precise delay with respect to a periodic digital input signal, comprising:
 means for providing a periodic digital input signal of a reference frequency;
 variable delay means for receiving the input signal and generating an output signal which is delayed with respect to the input signal; and
 phase-lock control means for receiving the input signal and the output signal and controlling the delay means so that the output signal is locked in phase with respect to the input signal.

13. The circuit of claim 12 wherein the control means includes means for causing the output signal to be delayed by a predetermined number of periods of the input signal.

14. The circuit of claim 12 or 13 wherein the control means includes:

- a phase comparator for comparing the phase of the input signal with the phase of the output signal and generating a first error signal when the phase of the input signal leads the phase of the output signal and a second error signal when the phase of the input signal lags the phase of the output signal; and

- correction means for generating a control signal in response to the error signals to control the amount of delay of the delay means.

15. The circuit of claim 14 wherein the correction means includes a charge pump having a capacitor which is charged in a first direction in response to the first error signal and in a second direction in response to the second error signal, wherein the voltage across the capacitor is the control signal for controlling the delay means.

16. The circuit of any of claims 12 to 15 wherein the delay means includes a plurality of series connected inverters and means for varying the switching speed of the inverters thereby to vary the delay of the delay means.

17. The circuit of claim 16 wherein each inverter is comprised of a pair of CMOS transistors the means for varying includes a plurality of first supply transistors coupled between a first power supply connection and the inverters for controlling the application of current to the inverters, wherein the supply transistors are driven by the control signal from the capacitor.

18. The circuit of claim 17 wherein:
 the means for varying includes a plurality of second supply transistors coupled between a second power supply connection and the inverters for controlling the application of current

to the inverters; and

the correction means includes means for generating a second control signal to drive the second supply transistors.

19. The circuit of claim 18 wherein the first supply transistors are MOS transistors of first conductivity type and the second supply transistors are MOS transistors of second conductivity type and wherein the means for generating the second control signal controls the value of the second control signal as a function of the value of the first control signal.

20. The circuit of claim 18 and 19 wherein the means for generating the second control signal includes:

- a first control MOS transistor driven by the control signal;
 a second control MOS transistor;
 a second capacitor connected to the gate of the second control MOS transistor, wherein the voltage on the second capacitor is the second control signal; and
 current control means for driving the second control MOS transistor so that the current through it has a predetermined relationship to the current through the first control MOS transistor.

21. The circuit of claim 20 wherein the current control means includes:

- a CMOS inverter having its input connected to its output, wherein the first and second control MOS transistors are connected to supply current to the inverter; and
 comparison means for comparing the output of the inverter to a reference voltage and driving the second control MOS transistor until the output of the inverter is equal to the reference voltage.

22. The circuit of claim 21 wherein the reference voltage is approximately equal to the switching voltage of the inverter.

23. A circuit for providing a controlled amount of delay to a digital input signal, comprising:

- reference frequency means for providing a periodic output signal;

- a first variable delay circuit for receiving the output of the reference frequency means and providing an output signal having a delay determined by a control signal;

- phase lock means for comparing the phase of the output signal of the reference frequency means with the phase of the output signal of the variable delay circuit and generating the control signal to the variable delay circuit which causes the output of the variable delay circuit to lock onto the phase of the output of the reference frequency means; and

- a second variable delay circuit for receiving a digital input signal and providing an output signal which is delayed with respect to the input signal, wherein the control signal is applied to the second delay circuit to control the amount of delay and wherein the variation in delay of the first delay circuit in response to a

change in the control signal is proportional to the change in the amount of delay of the second delay circuit in response to the same change in the control signal.

- 5 24. A phase-locked loop circuit for providing a signal which is precisely delayed with respect to a periodic reference signal, comprising:
- 10 a reference frequency source for providing the periodic reference signal;
a variable delay circuit having a first input for receiving the reference signal and a control input for receiving a control signal, the delay circuit providing a periodic output signal which
- 15 has the same frequency as the reference signal and is delayed with respect to the reference signal by an amount determined by the control signal;
- 20 control means for comparing the phase between the reference signal and the output signal and providing the control signal to the delay circuit to vary the amount of delay to achieve a desired phase relationship, the control means including means for determining
- 25 the direction of phase error between the reference signal and output signal and varying the control signal in a direction which will reduce the phase error.
- 30 25. A circuit as in claim 24 wherein the control means includes means for setting the control signal to an initial value which will result in a delay that causes the initial phase error to be in a known direction.
- 35 26. A circuit as in claim 23 and 24 wherein the control means includes:
- a phase detector for comparing the phases of the reference signal and the output signal and generating a first error signal when a phase error of a first direction is detected and
- 40 a second error signal when a phase error of a second direction is detected; and
- a charge pump for receiving the error signals and generating the control signal in response to the error signals.
- 45 27. A circuit as in claim 24, 25 or 26 wherein the phase detector includes:
- a first D-type flip-flop clocked by a rising edge of the reference signal;
- 50 a second D-type flip-flop clocked by a rising edge of the output signal;
- phase comparison control means for enabling the flip-flops in response to a first rising edge of the reference signal whereby the first flip-flop may be clocked by the next rising edge of the reference signal and the second flip-flop may be clocked by the next rising edge of the output signal; and
- 55 logic means connected to the outputs of the flip-flops for generating the error signals.
- 60 28. A circuit as in claim 27 wherein the phase comparison control means includes a third D-type flip-flop clocked by a rising edge of the reference signal, wherein the output of the third flip-flop controls the enabling of the
- 65 first and second flip-flops.

29. A circuit as in claim 28 wherein the third flip-flop is configured to provide an output which (a) enables the first and second flip-flops in response to a first rising edge of the reference signal to permit the first flip-flop to be clocked by the next rising edge of the reference signal and (b) resets the first and second flip-flops to a non-enabled condition in response to a third rising edge of the reference signal occurring immediately after said next rising edge of the reference signal.

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FILED

SPECIAL VERDICT FORM

APR 24 2006

RICHARD W. WICKING
CLERK, U.S. DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN JOSE

A. Instructions

For purposes of these questions, Rambus Inc. shall be referred to as "Rambus," and Hynix Semiconductor, Inc., Hynix Semiconductor America, Inc., Hynix Semiconductor U.K. Ltd. and Hynix Semiconductor Deutschland GmbH shall be referred to as "Hynix."

The questions below contain legal terms that are defined and explained in detail in the Jury Instructions. Please refer to the Jury Instructions if you are unsure about the meaning or usage of any legal term that appears in the questions below.

B. Findings on Rambus's Allegations of Patent Infringement by Hynix

1. Has Rambus proven that it is more likely than not that Hynix's SDRAM products infringe any of the following claims of Rambus's patents?

Answer "Yes" or "No" as to each claim:

'918 Patent, Claim 24 Yes ("yes" = infringed; "no" = not infringed)

'916 Patent, Claim 9 Yes

'916 Patent, Claim 28 Yes

2. Has Rambus proven that it is more likely than not that Hynix's DDR SDRAM products infringe any of the following claims of the Rambus patents?

Answer "Yes" or "No" as to each claim:

'105 Patent, Claim 34 Yes ("yes" = infringed; "no" = not infringed)

'918 Patent, Claim 24 Yes

'918 Patent, Claim 33 Yes

'020 Patent, Claim 32 Yes

'020 Patent, Claim 36 Yes

'916 Patent, Claim 9 Yes

'916 Patent, Claim 28 Yes

'916 Patent, Claim 40 Yes

C. Findings on Hynix's Allegations of Invalidity of Rambus's Patents

3. Has Hynix proven that it is highly probable that any of the following claims of Rambus's patents are invalid because the claims are "anticipated"?

Answer "Yes" or "No" with respect to each claim:

'918 patent, Claim 24 NO ("yes" = anticipated; "no" = not anticipated)

'120 ~~'102~~ patent, Claim 33 NO

'020 patent, Claim 32 NO

'020 patent, Claim 36 NO

'916 patent, Claim 9 NO

'916 patent, Claim 28 NO

'863 patent, Claim 16 NO

4. Has Hynix proven that it is highly probable that any of the following claims are invalid because the claimed invention would have been obvious at the time the invention was made to a person having ordinary skill in the art?

Answer "Yes" or "No" as to each claim:

'105 Patent, Claim 34 NO ("yes" = obvious; "no" = not obvious)

'918 Patent, Claim 24 NO

'918 Patent, Claim 33 NO

'120 Patent, Claim 33 NO

'020 Patent, Claim 36 NO

'916 Patent, Claim 9 NO

'916 Patent, Claim 28 NO

'916 Patent, Claim 40 NO

'863 Patent, Claim 16 NO

5. Has Hynix proven that it is highly probable that any of the following claims are invalid because the written description does not support the claim (i.e., does not satisfy the written description requirement)?

Answer "Yes" or "No" as to each claim:

'105 Patent, Claim 34 NO ("yes" = invalid because written description requirement not satisfied; "no" = not invalid because written description satisfied)

'918 Patent, Claim 24 NO

'918 Patent, Claim 33 NO

'120 Patent, Claim 33 NO

'020 Patent, Claim 32 NO

'020 Patent, Claim 36 NO

'916 Patent, Claim 9 NO

'916 Patent, Claim 28 NO

'916 Patent, Claim 40 NO

'863 Patent, Claim 16 NO

D. Findings on Rambus's Claim for Damages for Infringement [If Applicable]

6. If you have found a claim infringed and have not found that claim invalid, or you have found that either Claim 33 of the '120 patent or Claim 16 of the '863 patent is not invalid, then you are to find the damages which Rambus has proven that it more likely than not suffered as a result of Hynix's infringement. If you have not found a claim infringed and you have found that both Claim 33 of the '120 patent and Claim 16 of the '863 patent are invalid, then you have no further questions to answer, and you should proceed to Section E.

[If applicable] What damages has Rambus proven it more likely than not suffered as a result of infringement by Hynix's SDRAM product?

\$ 30,538,165

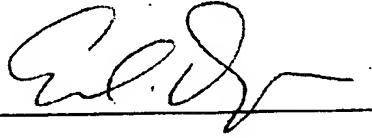
[If applicable] What damages has Rambus proven it more likely than not suffered as a result of infringement by Hynix's DDR SDRAM product?

\$ 276,429,107

E. Checking and Signing of Verdict Form

You have now reached the end of the verdict form and should review it to ensure it accurately reflects your unanimous determinations. The Presiding Juror should then sign and date the verdict form in the spaces below and notify the Security Guard that you have reached a verdict. The Presiding Juror should retain possession of the verdict form and bring it when the jury is brought back into the courtroom.

DATED: 4/24, 2006

By: 
Presiding Juror